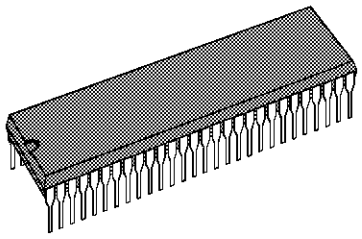
SGS-THOMSON MICROELECTRONICS

STV8230

NICAM SINGLE CHIP

ADVANCE DATA

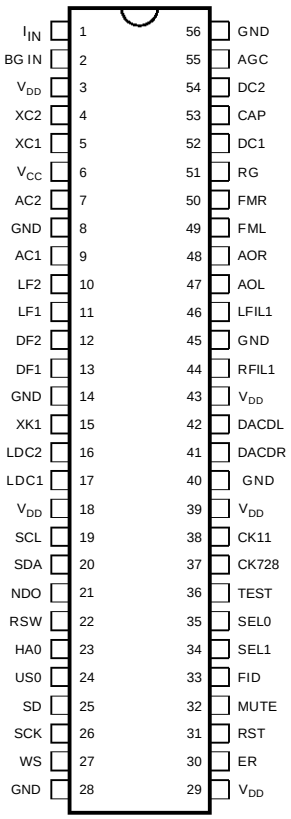
- DEMODULATION, DECODING and PROCESSING IN ONE CHIP
- ON CHIP DATA SHAPING AND FM NOTCH FILTERS
- AUTOMATIC DUAL STANDARD DEMODULATION
- SINGLE QUARTZ CRYSTAL FOR DUAL STANDARDS
- LANGUAGE AND SOURCE SELECTION SWITCH MATRIX
- STAND ALONE MODE OR I^2C BUS PROGRAMMABLE MODE
- PROGRAMMABLE ERROR MONITORING



SHRINK 56
(Plastic Package)

ORDER CODE : STV8230

PIN CONNECTIONS



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DESCRIPTION

The NICAM Single Chip STV8230, made in BICMOS technology, performs all the required processing for the NICAM signal, in accordance with EBU SPB 424 specifications. To save external components, data shaping filters and FM notch filters have been integrated. An I^2S output is provided for digital audio purposes and can be used as an input for converting to analog another digital source. The STV8230 can work in a stand alone mode by using some hardware configurable pins or in programmable mode by setting all functions via serial I^2C BUS.

PIN DESCRIPTION

Pin Name	Pin Number	Type	Functions
GENERAL			
VCC	6		++12V Supply
VDD	3,43		++5V Analog supply
VDD	18,39,29		++5V Digital supply
GND	8,45,56		Analog ground
GND	14,28,40		Digital ground
ANALOG			
IIN	1		System I input
BGIN	2		System B/G input
XC2	4		Optional carrier crystal system
XC1	5		Optional carrier crystal system
AC2	7		Data shaping filter output 2
AC1	9		Data shaping filter output 1
LF2	10		Clock recovery loop filter
LF1	11		Carrier recovery loop filter
DF2	12		Data filter 2 (eye monitor)
DF1	13		Data filter 1 (eye monitor)
XK1	15		Crystal oscillator (11.648MHz)
RFIL1	44		J17 de-emphasis right channel
LFIL1	46		J17 de-emphasis left channel
AOL	47		Audio output left
AOR	48		Audio output right
FML	49		FM audio left input
FMR	50		FM audio right input
RG	51		DAC gain resistor
DC1	52		Decoupling capacitor
CAP	53		Decoupling capacitor
DC2	54		Decoupling capacitor
AGC	55		AGC filter capacitor
DIGITAL			
LDC2	16	OUT	LED driver (stereo and data)
LDC1	17	OUT	LED driver (single and dual mono)
SCL	19	IN	IIC Serial bus clock
SDA	20	BIDIR	IIC Serial bus data
NDO	21	BIDIR	NICAM data
RSW	22	BIDIR	Reserve sound switch flag (force to FM)
HA0	23	IN	Chip address lsb
US0	24	OUT	User bit 0 (open drain)
SD	25	BIDIR	IIS Serial data
SCK	26	OUT	IIS Serial clock
WS	27	OUT	IIS Word select
ER	30	OUT	Error monitor
RST	31	IN	Power on reset
MUTE	32	BIDIR	Nicam mute (force to NICAM)
FID	33	OUT	Frame flag
SEL1	34	IN	Language selection 1
SEL0	35	IN	Language selection 0
TEST	36	IN	Test mode control
CK728	37	OUT	728KHz clock
CK11	38	BIDIR	11.648MHz clock
DACDR	41	BIDIR	DAC data right
DACDL	42	BIDIR	DAC data left

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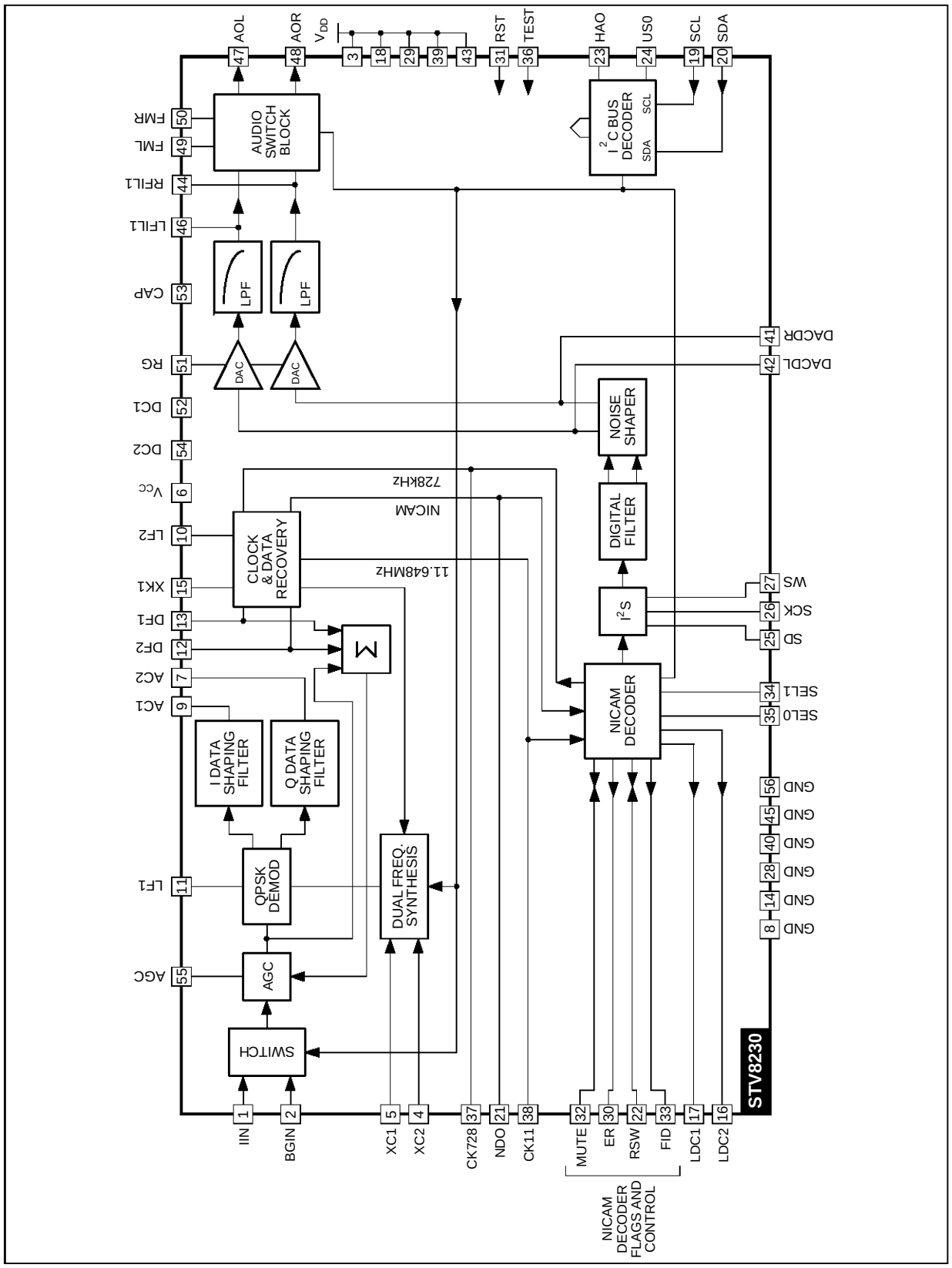
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The block diagram of the STV8230 shows that all the necessary functions required to accept the QPSK carrier and to derive from this the actual linear audio signals are contained entirely within the IC.

The two inter carrier inputs enter a source selection switch and pass immediately to an AGC block which has a total range of better than 40dB. The resulting levelled signal passes to the QPSK demodulator which recovers the NICAM 728Kb/s data stream by means of carrier and clock recovery circuits.

Carrier recovery is achieved with a baseband remodulator which consists of a phase locked loop with a switchable phase detector. This allows it to lock to one of four possible phases of the QPSK carrier without disruption due to the modulation. Dual frequency operation is made possible by synthesising the carrier reference frequency thus saving the need for two extra crystals.

The standards switch controls operation of the QPSK demodulator at either 6.552MHz or 5.85MHz. This can be controlled via the I^2C bus or the decoder set into automatic mode in which it determines the standard by alternately trying to lock to the two systems.

On chip switchable data shaping filters (40% Roll off cosine for B/G standard and 100% Roll off cosine for I standard) and FM notch filters save external components. Then the in-phase and quadrature data channels are sliced by comparators. The symbol clock is recovered from this data and used to sample and re-time it. The two data channels are then decoded and serialised to obtain the NICAM-728 data which is then passed on to the NICAM decoder.

The NICAM decoder performs data and sound recovery from the signals specified in EBU SPB 424. The expanded digital audio signals (14-bit) are made available at the digital audio interface in a serial multiplex of left and right channels. They are also processed by a 4-times upsampling digital filter and noise shaper which results in a high speed digital data stream which can be applied to the 1-bit D-A convertors.

Frame alignment to the NICAM signal requires searching out a Frame Alignment Word (FAW) and a 16 frames sequence conveyed by the C0 bit. This process is complicated by the presence of aliases of the FAW and, because of noise and interference, errors in the incoming NICAM data. A robust scheme is implemented which ensures the decoder will align, and stay aligned, to signals beyond the limit of maximum useable error rate (1-in-100).

All of the data in a NICAM frame is scrambled, expect for the FAW, to ensure randomising of the QPSK modulated carrier spectrum and to assist in clock recovery. A descrambler is contained in the STV8230 which generates a 511 bit PRBS which is synchronised to that used by the scrambler at the transmitter and performs modulo-2 addition with the incoming data. This recovers the original data.

For Pay-TV applications, alternative methods of encryption can be considered. One possible method is to change the initialisation of the PRBS generator on a frame-by-frame basis rather than having all nine bits of the PRBS set to 1 as is normally the case.

Such an encryption system can be managed in the STV8230. If 7 or less clock cycles are counted on CW-clock during a frame, then the PRBS is preset to all 1s. If 8 clock cycles are counted, 8 bits of CW-data are clocked into a shift register, the first bit of the last transfer now moving to bit-9 position in the shift register. The resulting value is used to preset the PRBS generator on the next frame. If 9 clock cycles are counted, the CW-data (which has been clocked into a 9-bit shift register) is used to preset the PRBS generator on the next frame. If 10 or more clock cycles are counted, only the first 9 bits of the CW-data are used and loaded into the PRBS generator on the next frame.

Together, a RAM and address generator de-interleave the incoming samples so that they are stored sequentially. NICAM frames are stored in three pages which allows simultaneous reading and writing of mono/stereo samples.

Scale factor bits are extracted from the samples by performing majority decision operations on the parity bits from groups of samples. This information is applied to the expander which shifts the 10-bit input samples to one of five positions thus forming a new 14-bit output word. Appropriate padding of missing LSB's and MSB's is provided.

Samples which are determined to be in error by the parity check are replaced by interpolated samples obtained from known good samples. Under high error rate or fault conditions, the samples are muted (set to all 0's).

An error counter provides muting for the NICAM audio if the error rate exceeds 1-in-100. To prevent chatter under marginal conditions, hysteresis is provided so that the audio will only un-mute if the error rate drops below 1-in-400.

An error output (ER) is provided which gives an indication of the BER by providing one pulse for every error in the data. This may be interpreted externally to give a representative indication for production line test purposes. The BER information is additionally available through the I^2C bus.

Majority decision logic recovers the application control information by decision over 16 frames. Flags are provided from here which indicate the mode of operation eg STEREO/MONO/DATA etc.

Language selection can be programmed through the SEL0/1 pins as in the following table :

SEL0	SEL1	L	R
0	0	M1	M2
0	1	M1	M1
1	0	M2	M2
1	1	M2	M1

In most cases, these pins will be set to 0 and language selection performed by the switch matrix in the audio processor.

Note that, in dual language operation, if M1 and M2 are selected and the NICAM signal fails, if reserve sound is available, M1 will default to the reserve sound and M2 will be muted.

A digital filter performs 4x upsampling in two stages. The main FIR 2x upsampler is followed by a smaller 2x FIR upsampler. Digital upsampling means a much simpler post-DAC reconstruction filter can be used thus saving on external component count and cost.

A noise shaper converts the samples from the digital filter into two high speed serial bit streams which can be applied to the DACs.

Conversion of the pulse density modulated bit streams to analog takes place and is followed by low pass filtering which removes high frequency quantising noise and performs J-17 de-emphasis. The DAC signal level can be adjusted to match that of the reserve sound by adjusting the value of RG up to a maximum of $1V_{RMS}$ on pins L/RFIL1.

Once the analog audio has been recovered, certain source switch functions must be performed. The reserve sound switch automatically selects FM-Mono/Stereo if the NICAM signal fails and the reserve sound flag (C4) is set to 1. If C4 is set to 0, the switch will not change and the audio outputs will be muted. If the NICAM signal only carries data, FM is selected. This switch can be forced to select FM via the I^2C bus in the case of marginal reception of the NICAM signal. Also, it can be forced to select a stereo audio signal from a Zweiton decoder for instance.

The audio outputs can be muted and an additional +6dB gain applied to raise the output levels to 1Vrms maximum. The DAC outputs are automatically mute under the following conditions :

1. Loss of frame alignment.
2. The bit error rate (BER) is >1-in-100.
3. The NICAM signal is conveying M1. The right DAC is muted unless M1 has been selected to be on both DAC outputs.
4. The NICAM signal is conveying data only.

A I^2C bus interface provides access to control and status registers within the chip to allow control of its functions and monitoring of status. A digital filter is included which improves noise immunity.

A standard configuration at power-on reset sets all the control register in a stand alone mode.

Thanks to this stand alone mode the STV8230 can work without any I^2C programmation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
V_{CC}	Supply Voltage	7	V
P_{tot}	Total Power Dissipation	1.2	W
T_{oper}	Operating Temperature Range	0, +70	^oC
T_{stg}	Storage Temperature Range	-20, +150	^oC

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	TBD	$^oC/W$

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ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_{CC} = 12V, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
SUPPLY					
V_{CC1}	Supply Voltage Range	11.4	12	12.6	V
V_{DD}	Supply Voltage Range	4.75	5	5.25	V
I_{CC}	Supply Current		40		mA
I_{DD}	Supply Current		80		mA
OUTPUTS					
SCK,WS,FID,CK728,CK11,NDO,ER					
V_{OL}	Low Output Voltage (I_{OL} = - 4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 4mA)	$0.7V_{DD}$			V
US0 (Open drain)					
V_{OL}	Low Output Voltage (I_{OL} = - 4mA)			0.4	V
I_{LK}	High Output Current (Leakage)			± 2	V
LED DRIVERS LDC1,LDC2					
I_{OL}	Low Output Current (V_{OL} = 0.4V)		- 4		mA
I_{OH}	High Output Current (V_{OH} = $0.7V_{CC}$)		+4		mA
INPUTS					
HAO,SEL1,SEL0,TEST,RST					
V_{IL}	Low Input Voltage			0.8	V
V_{IH}	High Input Voltage	$0.6V_{DD}$			V
I_{LK}	Input Leakage Current			± 2	µA
BI-DIRECTIONAL					
RSW, MUTE					
V_{OL}	Low Output Voltage (I_{OL} = - 4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 100µA)	$0.7V_{DD}$			V
V_{IL}	Low Input Voltage			0.8	V
SD, DACDL, DACDR					
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 4mA)	$0.7V_{DD}$			V
V_{IL}	Low Input Voltage			0.8	V
V_{IH}	High Input Voltage	$0.6V_{DD}$			V
I_{LK}	Input Leakage Current			± 2	µA
I^2C INTERFACE					
SCL					
V_{IL}	Low Input Voltage	0		1.5	V
V_{IH}	High Input Voltage	3		V_{DD}	V
f_{SCL}	SCL Clock Frequency			100	kHz
t_R, t_F	Input Rise/Fall Times			2	µs
I_{IL}	Input Leakage Current (V_1 = 5.5V with output off)			10	µA
C_I	Input Capacitance			7	pF

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ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_{CC} = 12V, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
I^2C INTERFACE					
SDA					
V_{IL}	Input Low Voltage	0		1.5	V
V_{IH}	Input High Voltage	3		V_{DD}	V
t_R, t_F	Input Rise/Fall Times			2	µs
I_{LK}	Input Leakage Current (V_1 = 5.5V with output off)			10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0		0.5	V
t_F	Output Fall Time between 3.0V and 1.0V			200	ns
C_L	Load Capacitance			400	pF
ANALOG PINS					
I-B/G SELECTOR					
Vdc	DC Bias Voltage		2.8		V
Rin	Input Resistance (Selected input)		10		kΩ
Cin	Input Capacitance		10		pF
AGC					
V_{IN}	Input Voltage Range (FM + NICAM carriers)			1000	mV_{PP}
AGCdyn	AGC dynamic range (NICAM to FM carrier ratio 7dB B/G system)		33		dB
AGCdyn	AGC dynamic range (NICAM to FM carrier ratio 10dB I system)		30		dB
AGClv	AGC Low Voltage (V_{IN} = max)		2		V
AGChv	AGC High Voltage (V_{IN} = min)		11		V
AGCta	AGC Attack Time (V_{IN} = min to max, CAGC = 100nF)		15		ms
AGCtd	AGC Decay Time (V_{IN} = max to min, CAGC = 100nF)		220		ms
QPSK DEMODULATOR (LF1)					
V_{DC}	DC Bias Voltage (SYN = 1)	1	5	10	V
Kd	Phase Detector Constant (no mod.)		33		µA/rad
Kv	VCO Constant		3.5		MHz/V
EYE DIAGRAM MONITORS (DF1, DF2)					
V_{DC}	DC Bias Voltage		2.5		V
R_{IN}	Input Resistance		10		kΩ
V_{IN}	Input Voltage (System I)		0.6		V_{PP}
CLOCK AND DATA RECOVERY (LF2)					
V_{DC}	DC Bias Voltage		2.5		V
Kd	Phase Detector Constant (all 1's)		3		µA/rad
Kv	VCXO Constant		4.29		kHz/V
DAC AND FILTER (LFIL1,RFIL1)					
V_{DC}	DC Bias Voltage		2.5		V
I_{OUT}	Output Current (R_G = 5.6kΩ ,DAC full scale)		340		$µA_{PP}$
V_{RG}	RG Pin DC Voltage		1.25		V
R_G	Gain adjustment Resistor	5.6		10	kΩ

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ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_{CC} = 12V, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
ANALOG PINS (continued)					
AUDIO OUTPUT (AOL,AOR)					
	DAC SELECTED				
V_{OUT}	Output Voltage (1kHz at -11.75dB,J17 de-emphasis, R_G = 5.6kΩ)		0.5		V_{RMS}
S/N	Relative to 0.5V_{RMS}, noise measured with IEC-179 A-filter		80		dB
THD	1kHz at 0.5V_{RMS}, R_G = 5.6kΩ		0.03		%
	Crosstalk at 1kHz, 0.5V_{RMS}		70		dB
Chm	Maximum Channel Matching Error			2	dB
	FM STEREO AUDIO INPUT SELECTED (FMR,FML)				
S/N	Relative to 0.5V_{RMS}, noise measured with IEC-179 A-filter		88		dB
THD	1kHz at 0.5V_{RMS}		0.02		%
	Crosstalk at 1kHz, 0.5V_{RMS}		80		dB
Chm	Maximum Channel Matching Error			2	dB
	FM AUDIO INPUT				
V_{IN}	FM Signal Input Voltage		0.5	1.2	V_{RMS}
V_{DC}	DC Bias Input Voltage		2.5		V
I^2C BUS TIMING					
SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)					
t_{LOW}	Low Period Clock	4			µs
t_{HIGH}	High Period Clock	4			µs
$t_{SU,DAT}$	Data Set-up Time	250			ns
$t_{HD,DAT}$	Data Hold Time	170			ns
$t_{SU,STO}$	Stop Set-up Time from Clock High	4			µs
t_{BUF}	Start Set-up Time following a Stop	4			µs
$t_{HD,STA}$	Start Hold Time	4			µs
$t_{SU,STA}$	Start Set-up Time following Clock Low to High Transition	4			µs

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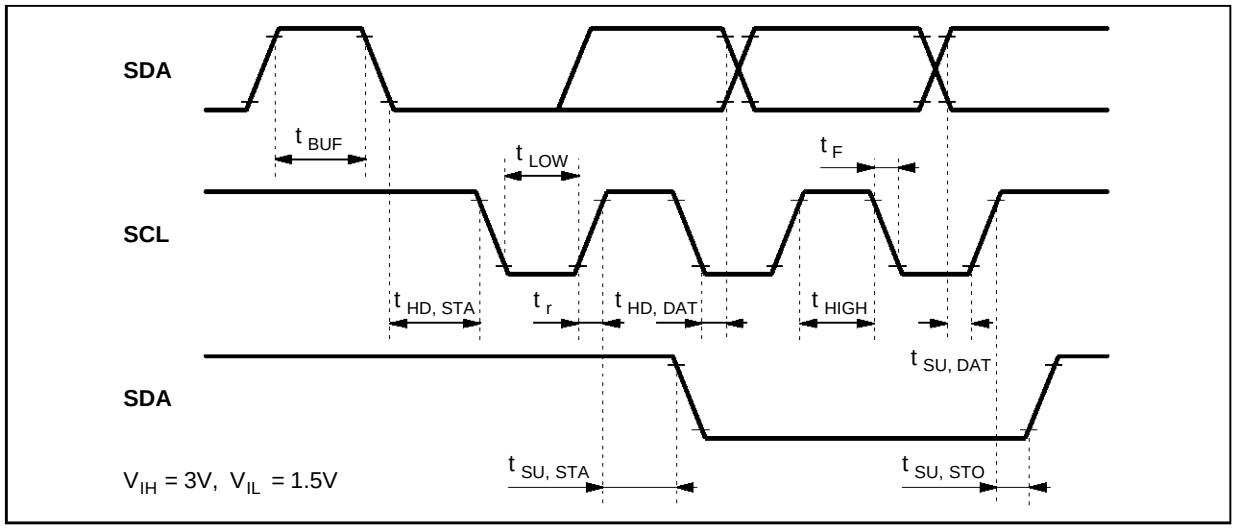
Figure 1 : I^2C Bus Timing



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I²C REGISTERS

Software control of IC's is given by programming four registers, one read only status register (SR0) and three read and write control registers (CR1,CR2,CR3).

Transmit format : S=Start, A=Acknowledge, P=Stop

S	CHIP ADDRESS	0	A	REG SUB ADDRESS	A	DATA	A	P

Receive format :

S	CHIP ADDRESS	1	A	SR0 DATA	A	CR1 DATA	A	P

Note : "All registers are read sequentially; device status and the contents " of all registers may be read. The sequence may be terminated by not acknowledging (NOACK) the slave.

Chip address

1	0	1	1	0	1	HAO	R/W

MSB LSB

HAO : Hardware address selection pin

Register addresses

Reg. Name	Sub Address								Function
SR0	0	0	0	0	0	0	0	0	NICAM status
CR1	0	0	0	0	0	0	0	1	Filters & Audio switch control
CR2	0	0	0	0	0	0	1	0	NICAM control
CR3	0	0	0	0	0	0	1	1	System control

SR0 : NICAM status (read only)

STD	C1	C2	C3	C4	MUT	LA2	L/S
0	0	0	0	1	1	1	1

MSB LSB

STD : STandard selecteD, 0 = system I, 1 = system B/G
C4 : Reserve sound flag, 1 = FM back up
C1-C3 : Application bits received after majority logic
MUT : Nicam MUTe, 1 = DAC output muted
LA2 : 1 = lost of super frame alignment
L/S : if FN1 = 0 then Loss of frame alignment if L/S = 1
: if FN1 = 1 then L/S = STD (L/S = 1, B/G standard - L/S = 0, I standard)

CR1 : Filters and Audio Switch control (read and write register)

X		X	FL2	FL1	FL0	G0	AUM	FRE
0	0	0	0	0	0	0	0	

MSB LSB

FLn : Filter control
FL2 = 0, Root cosine filter enabled
FL1 = 0, I or B/G notch filter enabled
FL0 = 0, B/G group delay equalizer disabled
G0 : Audio buffer gain, 0 = 0dB, 1 = +6dB
AUM : Audio mute, 1 = muted
FRE : Free run clock VCXO FOR SET UP ON LF2, 1 = free run

CR2 : NICAM control (read and write register)

SDI	ECT	MAE	FN1	UMT	LA1	LA0	X
0	0	0	0	0	0	0	1

MSB LSB

SDI : I^2S interface direction - 0 = Output, 1 = Input
ECT : Bit error rate counting time - 0 = 128ms, 1 = 64ms
MAE : Max allowed errors - 0 = 511, 1 = 255
FN1 : Set function of bit 0 in SR0 (status register)
0 = loss of frame alignment, 1 = standard status (I or B/G)
UMT : Un-mute NICAM, 1 = force to un-mute, 0 = automatic
LA1 : Language select 1 (LA1 + SEL1) (see Figure 3)
LA0 : Language select 0 (LA0 + SEL0) (see Figure 3)

ECT	MAE	BER MUTE
0	0	8.9 x 10-3 (1 in 112)
0	1	4.4 x 10-3 (1 in 225)
1	0	1.8 x 10-2 (1 in 56)
1	1	8.9 x 10-3 (1 in 112)

C3	C2	C1	LDC1	LDC2	MODE
0	0	0	Z	0	Stereo
0	1	0	0	Z	Dual Mono
0	0	1	1	Z	Single mono
0	1	1	Z	1	Data
1	X	X	Z	Z	-

Z = High impedance

CR3 : System control (read and write register)

X	US0	AUT	IBG	FS1	FS0	X	SYN
0	0	1	0	0	0	0	1

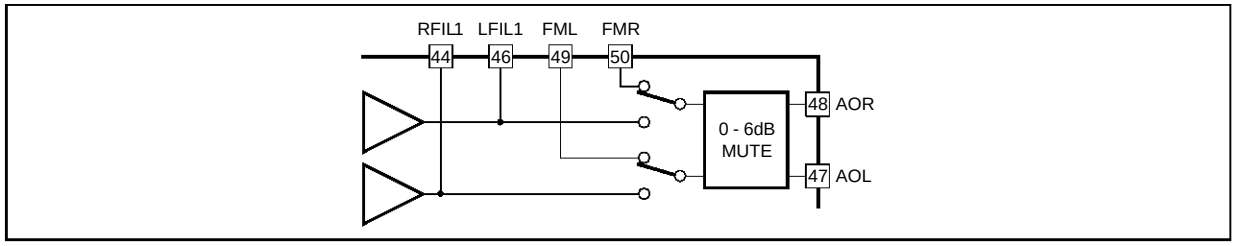
MSB LSB

US0 : User bit 0 (output)
AUT : Automatic standard selection, 1 = enable
IBG : Standard select when AUT =0, 1 = B/G, 0 = I
FSn : Force setting of reserve sound switch (see table and Figure 2)
SYN : 1 = synthesiser, 0 = dual VCXO (carrier loop)

FS1	FS0	Selection
0	0	Auto NICAM
0	1	FM-Stereo
1	0	FM-Stereo
1	1	NICAM

@ Register configuration on power on reset and in stand alone mode X bit must not be used. To be left at power on reset value

Figure 2 : Audio Switches Selection



NICAM STAND-ALONE APPLICATION

The NICAM single chip has been designed to be monitored by the I^2C bus; nevertheless stand-alone working capability is offered to the designer for low cost applications.

In order to know the status of the device in stand-alone mode, consider the content (@) of the four I^2C registers at power-ON (4 registers : SR0 - CR1 - CR2 - CR3).

Hardware configuration pins are described below.

RSW (Pin 22)

- as an output :
  status of the RSW switch
  - 0 = FM stereo
  - 1 = NICAM
- as an input
  - 0 = FM stereo (forced)

SEL0 /SEL1 (PINS 34/35) (see Figure 3)

- to select the language in case of bilingual operation.
- selected value is related to LA0 and LA1

As the I^2C bus is not used LA0 and LA1 = 0 (power-on condition)/ SEL0 = Q0, SEL1 = Q1

The 4 choices are summarized in the table below.

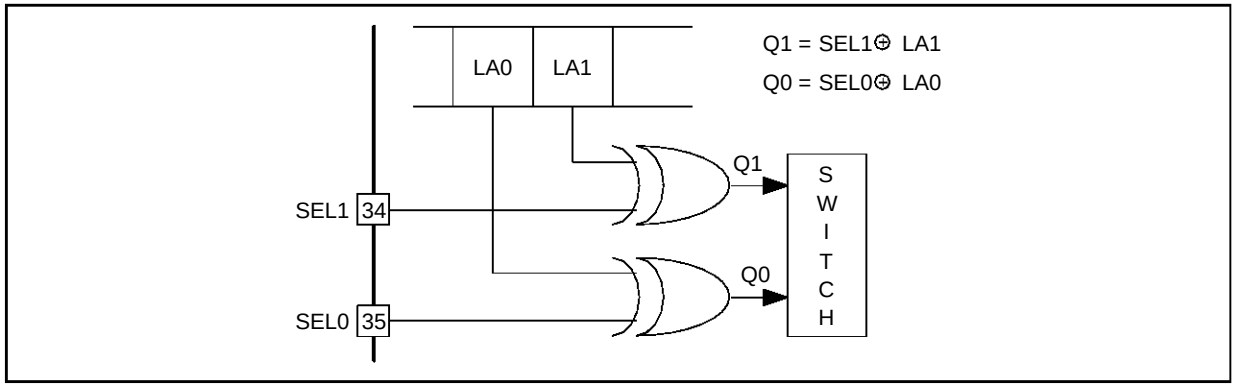
SEL0	SEL1	DACDL	DACDR
0	0	M1	M2
0	1	M1	M1
1	0	M2	M2
1	1	M2	M1

M1 = Mono 1
M2 = Mono 2

MUTE (PIN 32)

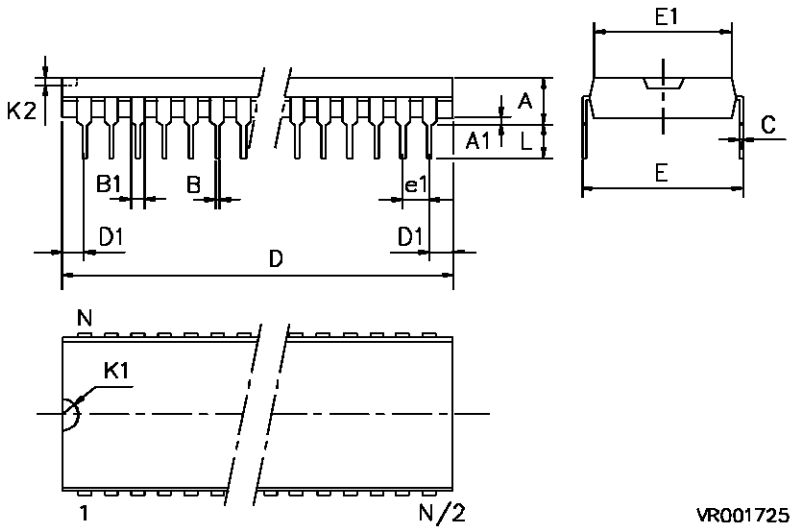
- as an output :
  status of the DAC
  - 0 = unmuted
  - 1 = muted
- as an input :
  - 0 = unmute DAC (forced)

Figure 3 : Langage Selection



PACKAGE MECHANICAL DATA

56 PINS - PLASTIC SHRINK DIP



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Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	–	–	–	–	–	–
E			18.54			0.730
E1		13.72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2.54		3.81	.100		0.150
e1		1.78			0.070	

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